Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.106”**

**.120”**

**G**

**SOURCE**

**Chip back is Drain**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: G = .021” X .025”**

**Backside Potential: Drain**

**Mask Ref: GEN 5**

**APPROVED BY: DK DIE SIZE .106” X .120” DATE: 9/22/21**

**MFG: INT’L RECTIFIER THICKNESS .015” P/N: IRFC9130N**

**DG 10.1.2**

#### Rev B, 7/19/02